The opinion in support of the decision being entered today was ***not*** written for publication and is ***not*** binding precedent of the Board

Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte PATRICK YIN

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Appeal No. 1999-0007
Application 08/688,218

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ON BRIEF

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Before HECKER, LALL and BLANKENSHIP, ***Administrative Patent Judges***.

HECKER, ***Administrative Patent Judge.***

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 3 through 6, 9 through 13, 18 and 19, all claims pending in this application.

The invention relates to taking an integrated circuit that is designed for one manufacturing process and implementing the circuit in a new manufacturing process. In particular, an

integrated circuit is generated essentially from the libraries (i.e., databases) associated with the integrated circuit and the place and route information. In doing so, a Netlist Database, a Place and Route Database and a Physical Database can be generated therefrom that can be readily implemented into a physical integrated circuit. When a new manufacturing process is utilized to generate a new integrated circuit, the only things that need to be done are a mapping of the physical cell library, generating new timing models, and finally mapping the Place and Route Database.

Representative independent claim 18 is reproduced as follows:

18. A method for taking a first integrated circuit from a first manufacturing process and generating a second integrated circuit from a second manufacturing process comprising the steps of:

(a) providing a first plurality of libraries from the first integrated circuit, the first plurality of libraries including a timing library, a logic cell library, a place and route cell library and a physical cell library; the first plurality of libraries defining characteristics of the first integrated circuit including routing grid dimensions of the first integrated circuit, the routing grid dimensions of the first integrated circuit being defined by a grid where signal interconnections and cells are placed; and being definable by layout design rules of the first manufacturing process;

(b) mapping the physical cell library based on layout design rules of the second manufacturing process, the layout design rules of the second manufacturing process defining routing grid dimensions for the second integrated circuit;

(c) characterizing the physical cell library and producing a timing library based upon a plurality of device models of the second manufacturing process;

(d) generating a second plurality of libraries including a place and route library; the second plurality of libraries defining characteristics of the second integrated circuit; and

(e) utilizing a place and route database of the first manufacturing process and the routing grid dimensions of the first manufacturing process to map into a second place and route data base of the second manufacturing process; the place and route database of the second manufacturing process providing routing grid dimensions in such a manner that the position of the cell placements and inter-connections are relatively the same as in the first manufacturing process; the second place and route database defining the second integrated circuit.

The Examiner relies on the following references:

Upton et al. (Upton)	5,351,197	Sept. 27, 1994
Dai et al. (Dai)	5,452,239	Sept. 19, 1995

Claims 3 through 6, 9 through 13, 18 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Upton in view of Dai.[1]

[1] The Examiner notes an objection to the drawings (answer-unnumbered third page), however (continued...)

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the brief, reply brief and answer for the respective details thereof.

OPINION

After a careful review of the evidence before us, we will not sustain the rejection of claims 3 through 6, 9 through 13, 18 and 19 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l,***

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[1](...continued)
this issue is not before us.

Inc., 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995)(***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984)).

The Examiner reasons that Upton teaches generating a specific version of an integrated circuit by design rules corresponding to a first process technology. The Examiner asserts this would imply having a database for storing the design information. (answer-pages 2 and 3.) The Examiner states:

> If a version of the module is needed in a different rule set [i.e. different process technology], a design rule variable file containing these new values can be ***substituted*** for the original file corresponding to mapping data as claimed. This substituted file for the original file would be another database corresponding to a design process technology for a second manufacturing process. Thus data files would imply having databases for storing design information for different versions or different manufacturing processes. [answer-page 3.][Emphasis added.]

However, the Examiner notes, Upton does not explicitly mention that generating a new integrated circuit according to the process technology is accomplished through the use of a place and route

database. The Examiner notes that Dai teaches this feature, and that Figure 14 thereof shows two chip place and route items for data transformation, translation or mapping. The Examiner contends, since Upton suggests the use of substitution of files for different rule sets, incorporating the teachings of Dai using two chip place and route databases into Upton, one of ordinary skill in the art at the time the invention was made would have found it obvious to translate and characterize from one design process technology to another process technology environment. This would enhance design process for different manufacturing processes and save time and cost (answer-pages 3 and 4.)

Appellant argues that Upton fails to teach or suggest the ***translation*** of a first routing grid dimension to a second routing grid dimension via a place and route library and database. Any changes needed in Upton for different design rule sets are done via design rule variable file ***substitution*** (brief-page 13).

We agree with Appellant. Upton designs only one integrated circuit. There is no first and second integrated circuit in Upton. Upton selects the technology to be used and the design rule variables corresponding thereto (column 6, lines 44-60).

The geometry, simulation model and schematic symbol databases (i.e., libraries) are the embodiment of the integrated circuit being created (column 8, lines 44-53). Upton states:

> If a version of the module [integrated circuit] is needed in a different rule set, a design rule variable file containing these new values can be substituted for the original file. The module compiler **68** can produce the geometry simulation model, schematic symbol and transistor model generators (**65, 69, 67** and **70**, respectively) embodying the constraints as specified for any given design rule set. [Column 9, lines 26-32.]

Thus, Upton does not ***translate*** the databases embodying a first integrated circuit (of a first technology) to databases embodying a second integrated circuit (of a second technology). Rather, Upton ***substitutes*** a different rule set into the design program, and generates databases for an integrated circuit ab initio, ***not by translation*** from existing first integrated circuit databases.

Appellant further argues that Dai makes no teaching or suggestion that the place and route database is also used to map into another place and route database for a different manufacturing process (brief-page 14). Still further, Appellant argues, nothing in Dai teaches or suggests mapping between ***two***

place and route databases within a configuration database (brief-page 15). Additionally, Appellant contends that Dai's Figure 14 illustrates the ***use*** of ***one*** place and route element 112 ***twice*** in a flow diagram rather than ***two*** place and route elements 112 (reply brief-page 2).

We agree, Dai teaches the interconnections for an emulation circuit to ***emulate*** an integrated circuit (abstract). As such, logic chips 18 are interconnected via interconnect chips 20 (column 4, line 67 - column 5, line 4), using a place and route module 112 (column 22, lines 66-68). We see no motivation to use Dai's place and route module in Upton since Dai has nothing to do with any process technology. Dai merely establishes that place and route modules are known.

Furthermore, having reviewed the pertinent sections of Dai, columns 22-24, we agree with Appellant that only one place and route module is disclosed.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***,

972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing*** ***In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg. v. SGS Importers Int'l***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

As pointed out above, Upton does not teach the translation of first databases embodying an integrated circuit for a first manufacturing process, to second databases embodying the integrated circuit for a second manufacturing process. Upton teaches the generation of databases ***ab initio*** for an integrated circuit in different manufacturing processes. Dai generates an emulation circuit, and has nothing to do with manufacturing processes. Dai discloses a single place and route module and provides no motivation to use such in Upton. Since there is no evidence in the record that the prior art suggested Appellant's claimed invention, we will not sustain the Examiner's rejection.

We have not sustained the rejection of claims 3 through 6, 9 through 13, 18 and 19 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

Stuart N. Hecker Administrative Patent Judge	)	
Parshotam S. Lall Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
Howard B. Blankenship Administrative Patent Judge	)	

SNH/cam

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